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EXAMINER	
NGUYEN, HAI L	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/903,227	BELL, DEBRA M.	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49 and 74-84* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *41-49* is/are allowed.

6)☒ Claim(s) *1-4,6-14,16-19,22,23,25-27,30-38 and 74-84* is/are rejected.

7)☒ Claim(s) *5,15,20,21,24,28,29,39 and 40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/05/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment received on 08/02/04 has been reviewed and considered with the following results:

As to the objections to claim 47, Applicant's amendments have overcome the objections, as such; the objections have been withdrawn.

As to the rejections to the claims, under 35 U.S.C. 112, 2nd paragraph, Applicant's amendments have overcome the rejections, as such; the rejections have been withdrawn.

As to the prior art rejections to claims 41-49, Applicant's arguments with respect to the previous prior art rejections mailed on 03/29/04 have been considered and found persuasive, as such; the prior art rejections to claims 41-49 have been withdrawn.

As to the prior art rejections to claims 1-4, 6-14, 16-19, 22, 23, 25-27, 30-38, and 74-84, Applicant's arguments with respect to the prior art rejections by the previous office action mailed on 03/29/04 have been fully considered but are not deemed to be persuasive. Therefore, the prior art rejection is maintained. The arguments supporting the previous rejections are addressed in detail below.

Claim Objections

2. Claim 79 is objected to because of the following informalities: lines 5-6, "an clock internal signal" should be changed to --an internal clock signal--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-4, 6-14, 16-19, 22, 23, 25-27, 30-38, and 74-84 are rejected under 35 U.S.C. 102(e) as being anticipated by Hassoun et al. (US 6,587,534; previously cited).

With regard to claim 1, Hassoun et al. discloses in Figs. 3-8 a delay locked loop (DLL), comprising a delay line (310, 350) including an input for receiving an external clock signal (302), and multiple outputs for providing multiple delayed signals (P_CLK_1 – P_CLK_N-1) including a first delayed signal and a second delayed signals; a selector (340) connected to the multiple outputs for selecting the first delayed signal (one of the following signals P_CLK_1 – P_CLK_N-1) to provide an internal clock signal (S_CLK) such that the external and internal clock signals are synchronized; and a command react circuit (330) connected to the selector for enabling the selector to select the second delayed signal (another signals of the following signals P_CLK_1 – P_CLK_N-1) based on a first state of a command signal (308) to provide the internal clock signal and for enabling the selector to select the first delayed signal based on a second state of the command to provide the internal clock signal.

With regard to claim 2, the DLL further comprises a phase detector (320, 620) for comparing the external and internal clock signals to produce shifting signals; and a controller (330) connected to the delay line for adjusting an amount of delay applied to the external clock

signal based on the shifting signals when the external and internal clock signals are not synchronized.

With regard to claims 3 and 4, Hassoun et al. also meets the claimed limitations in these claims.

With regard to claims 6 and 74, Hassoun et al. discloses in Figs. 3-8 a delay locked loop (DLL), and a method of use thereof, comprising a plurality of delay stages (310, 350) for applying a first amount of delay to an external signal (302) to generate a first delayed signal and for applying a second amount of delay to the external clock signal to generate a second delayed signal; a selector (340); and a command react circuit (330), the command react circuit including a first input for receiving a command signal (308), a second input for receiving a phase detect signal (output signal of 320), and an output node responsive to the command and phase detect signals for providing a command set signal to enable the selector to provide the internal clock signal based on the second delayed signal when the command signal is activated (one of the logic levels Lo or Hi), and to provide the internal clock signal based on the first delayed signal when the command signal is deactivated (the other logic level).

With regard to claims 7-12, Hassoun et al. also meets the claimed limitations in these claims.

With regard to claim 13, Hassoun et al. discloses in Figs. 3-8 a delay locked loop (DLL), comprising a plurality of delay stages (310, 350) for applying a first amount of delay to an external signal to generate a first delayed signal (output signal of 730_2 or 730_3) and for applying a second amount of delay to the external clock signal to generate a second delayed signal (output signal of 730_1), wherein the second amount of delay is smaller than the first

amount of delay by a delay quantity; a selector (340) connected to the delay stages for receiving the first and second delayed signals to provide an internal clock signal such that the external and internal clock signals are synchronized; and a command react circuit (330), the command react circuit including a first input for receiving a command signal (308), a second input for receiving a phase detect signal, and an output node responsive to the command and phase detect signals for providing a command set signal to enable the selector to provide the internal clock signal based on the second delayed signal when the command signal is activated (one of the logic levels Lo or Hi), and to provide the internal clock signal based on the first delayed signal when the command signal is deactivated (the other logic level).

With regard to claims 14 and 16-19, Hassoun et al. also meets the claimed limitations in these claims.

With regard to claim 22, Hassoun et al. discloses in Figs. 3-8 a delay locked loop (DLL), comprising a plurality of delay stages (310, 350) for applying a first amount of delay to an external signal to generate a first delayed signal (output signal of 730_1) and for applying a second amount of delay to the external clock signal to generate a second delayed signal (output signal of 730_2 or 730_3), wherein the second amount of delay is greater than the first amount of delay by a delay quantity; a selector (340) connected to the delay stages for receiving the first and second delayed signals to provide an internal clock signal such that the external and internal clock signals are synchronized; and a command react circuit (330), the command react circuit including a first input for receiving a command signal (308), a second input for receiving a phase detect signal, and an output node responsive to the command and phase detect signals for providing a command set signal to enable the selector to provide the internal clock signal based

on the second delayed signal when the command signal is activated (one of the logic levels Lo or Hi), and to provide the internal clock signal based on the first delayed signal when the command signal is deactivated (the other logic level).

With regard to claims 23 and 25-27, Hassoun et al. also meets the claimed limitations in these claims.

With regard to claim 30, Hassoun et al. discloses in Figs. 3-8 a delay locked loop (DLL), comprising a plurality of delay stages (310, 350) for applying a first amount of delay to an external signal (302) to generate a first delayed signal and for applying a second amount of delay to the external clock signal to generate a second delayed signal; a selector (340); and a command react circuit (330), the command react circuit including a first input for receiving a command signal (308), a second input for receiving a phase detect signal (output signal of 320), and an output node responsive to the command and phase detect signals for providing a command set signal to enable the selector to replace the first delayed signal with the second delayed signal when the command signal is activated (one of the logic levels Lo or Hi) while the external and internal clock signals are synchronized (note that whether the external and internal clock signals are synchronized or not will not effect the operation of the command set signal to enable the selector to replace the first delayed signal with the second delayed signal), and enable the selector to replace the second delayed signal with the first delayed signal when the command signal is deactivated (the other logic level).

Claim 32 is similarly rejected; note the above discussion with regard to claim 2.

With regard to claims 31, 33-35, 37, 38, 75 and 76, Hassoun et al. also meets the claimed limitations in these claims.

With regard to claim 36, the DLL further comprises a phase detector (320) connected to the command react circuit (330) to provide the phase detect signal, and wherein the phase detector is configured to activate, wherein the phase detect signal when the external and internal clock signals are not synchronized (see column 6, line 59 through column 7, line 14).

Claims 77-78 are similarly rejected; note the above discussion with regard to claims 13 and 22.

With regard to claim 79, Hassoun et al. inherently discloses in Figs. 3-8 a method of operating a delay locked loop, comprising the steps of applying an amount of delay to an external clock signal to generate a first delayed signal and a second delayed signal (310, 350); selecting a signal (340) among the first and second delayed signals to generate an clock internal signal (S_CLK); adjusting the amount of delay until the external and internal clock signals are synchronized (see column 6, line 59 through column 7, line 14); and reducing the amount of delay by a delay quantity when a command signal (308) is activated (one of the logic levels Lo or Hi to select a delayed signal which having an amount of delay is smaller) while the external and internal clock signals are synchronized and before the external and internal clock signals are detected as out of synchronism.

With regard to claim 80, the method further comprises the steps of increasing the amount of delay by the delay quantity when the command signal is deactivated (the other of the logic level); and adjusting the amount of delay until the external and internal clock signals are synchronized (see column 6, line 59 through column 7, line 14).

With regard to claim 81, reducing the amount of delay (by setting 308 at one of the logic levels Lo or Hi to select a delayed signal which having an amount of delay is smaller) occurs

before a phase detect signal is activated, wherein the phase detect signal is activated when the external and internal clock signal are not synchronized (see column 6, line 59 through column 7, line 14).

Claims 82-84 are similarly rejected; note the above discussion with regard to claims 79-81.

Response to Arguments

5. Applicant's first argument with respect to the prior art rejections of claim 1 concerning that "Applicant is unable to find in Hassoun "a command react circuit connected to the selector for enabling the selector to select the second delayed signal based on a first state of a command signal to provide the internal clock signal and for enabling the selector to select the first delayed signal based on a second state of the command to provide the internal clock signal" " is not persuasive because all the limitations in this claim are clearly anticipated by the reference. For example, Figs. 3-8 of Hassoun et al. shows that a command react circuit (330) connected to the selector (340) for enabling the selector to select the second delayed signal (i.e., the output signal of 730-2) based on a first state (logic level Lo) of a command signal (308) to provide the internal clock signal and for enabling the selector to select the first delayed signal based on a second state (logic level Hi) of the command to provide the internal clock signal. In other words, when the command react circuit (330) are set to select the output signal of 730-2, which is from one of the input signals of 730-2 at the input terminals 0 and 1, depends on the first logic level of the command signal to select one of those input signals to provide as the internal clock signal; and then when the command signal is set at the second logic level (at a different logic level) the other

input signal of 730-2 will be selected. Therefore, the limitations in the claim are clearly anticipated by the reference.

6. Applicant's next arguments with respect to the prior art rejections of claims 6, 22, 30, 74, and 79 concerning the same issue. Based on the discussion above and the rejections to the claims above, under 35 U.S.C. 102(e), the reference clearly anticipates all the rejected claims.

Allowable Subject Matter

7. Claims 41-49 are allowed.

8. Claims 5, 15, 20, 21, 24, 28, 29, 39, and 40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose or fairly suggest a command react circuit (140 in instant Fig. 1 of present application) configured in a delay locked loop (DLL) circuit, as recited in claims 5, 20, 28, 39, and 41, comprises a specific structural limitations such as a first input for receiving a command signal (146), a second input for receiving a phase detect signal (145), and an output node responsive to the command and phase detect signals for providing a command set signal (122) to enable the selector to replace the first delayed signal (DLLCK0) with the second delayed signal (DLLCK1) when the command signal is activated (logic level Hi) while the external and internal clock signals (101, 155) are synchronized (144 is at logic level Hi), and to enable the selector to replace the second delayed signal with the first delayed signal when the phase detect signal is activated and the command signal is not activated.

The prior art of record fails to disclose or fairly suggest a delay locked loop (DLL) circuit, as recited in claims 15 and 24, comprises a plurality of delay stages (112 in instant Fig. 1); a selector (130) connected to the delay stages for receiving the first and second delayed signals (DLLCLK0, DLLCLK1) to provide an internal clock signal such that the external and internal clock signals are synchronized; a command react circuit (140), the command react circuit including a first input for receiving a command signal (146), a second input for receiving a phase detect signal (145), and an output node responsive to the command and phase detect signals for providing a command set signal (122) to enable the selector to provide the internal clock signal based on the second delayed signal when the command signal is activated, and to provide the internal clock signal based on the first delayed signal when the command signal is deactivated; a phase detector (150) for comparing the external and internal clock signals to produce shifting signals (142, 143); and specifically the limitation directed to a shift register (305 in instant Fig.3) for adjusting the first amount of delay and the second amount of delay based on the shifting signals when the external and internal clock signals are not synchronized (144 is at logic level Lo).

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

HLN
September 1, 2004

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800